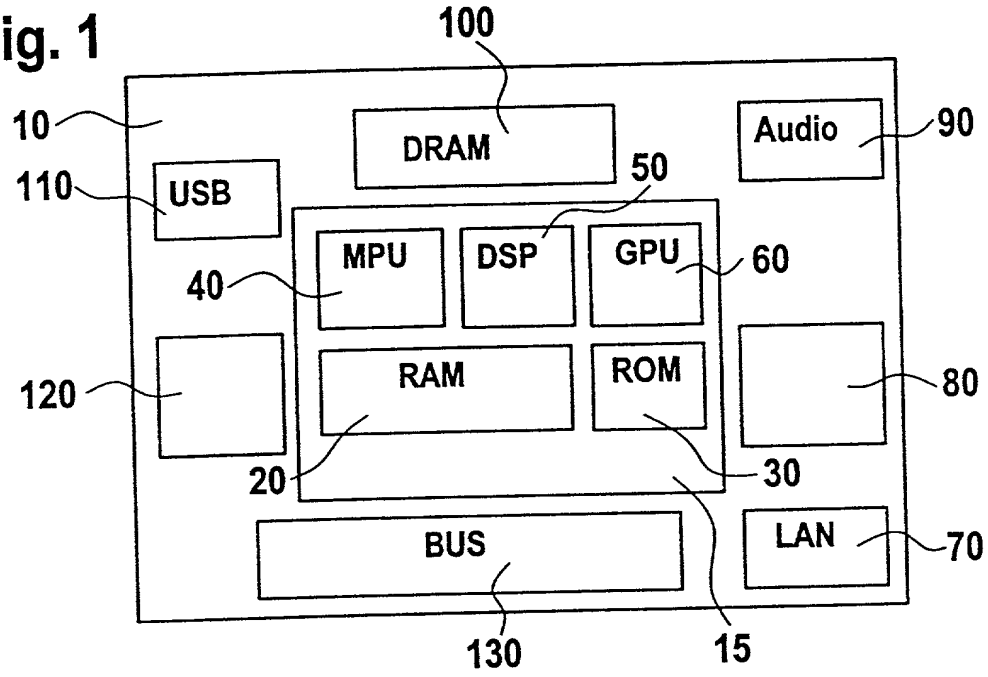
Fig. 1



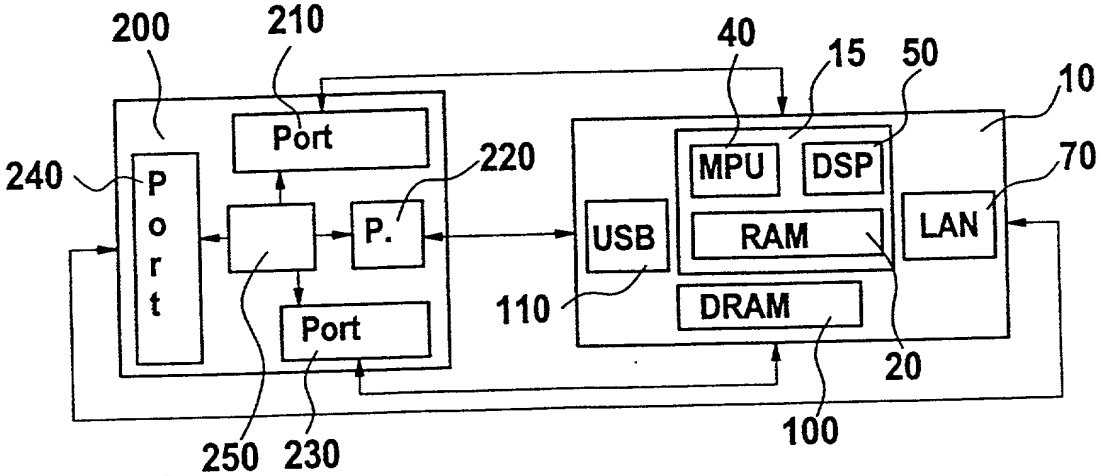


Fig. 2

Fig. 3

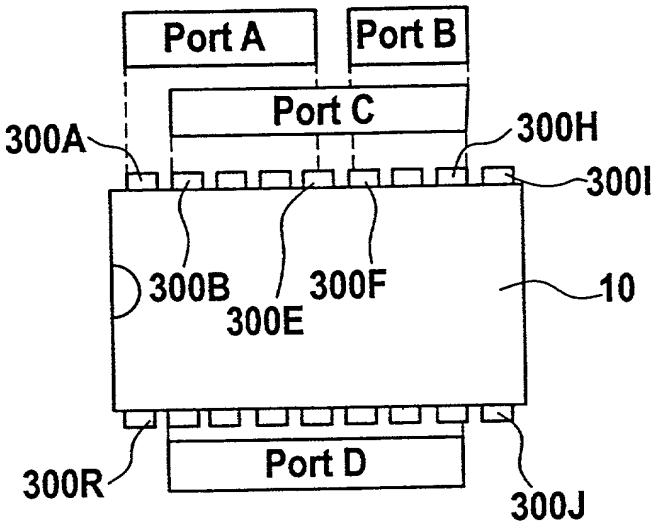

Port A
Port B
Port C
300A
300H
300I
300B
300E
300F
10
300R
Port D
300J

Fig. 4

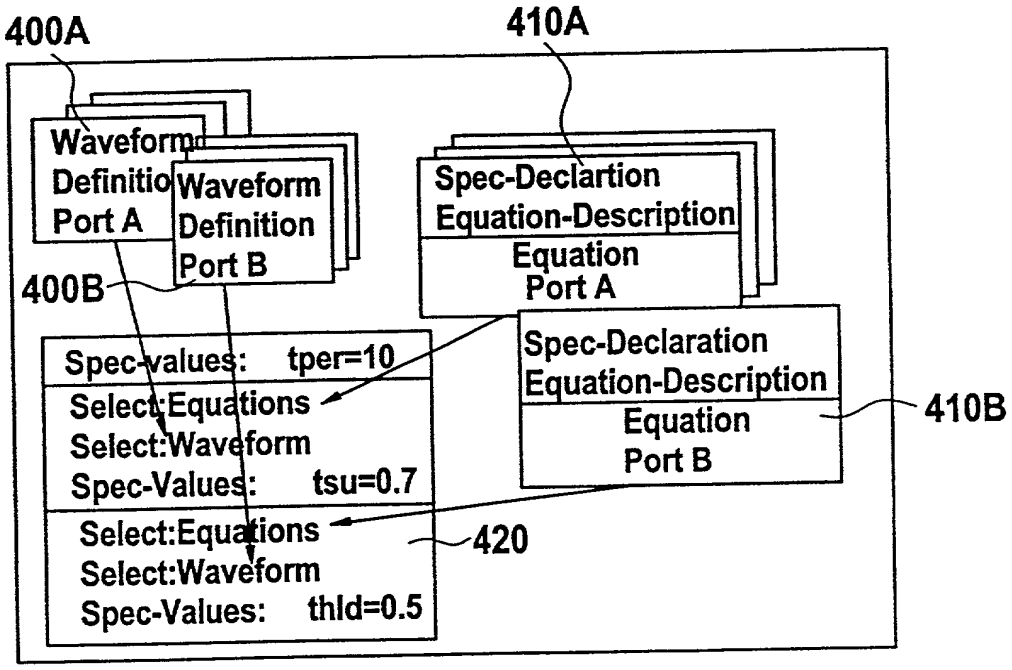

400A
410A
Waveform
Definitio
Port A
Waveform
Definition
Port B
400B
Spec-Declartion
Equation-Description
Equation
Port A
Spec-values: tper=10
Select:Equations
Select:Waveform
Spec-Values: tsu=0.7
Spec-Declaration
Equation-Description
Equation
Port B
410B
Select:Equations
Select:Waveform
Spec-Values: thld=0.5
420

Fig. 5

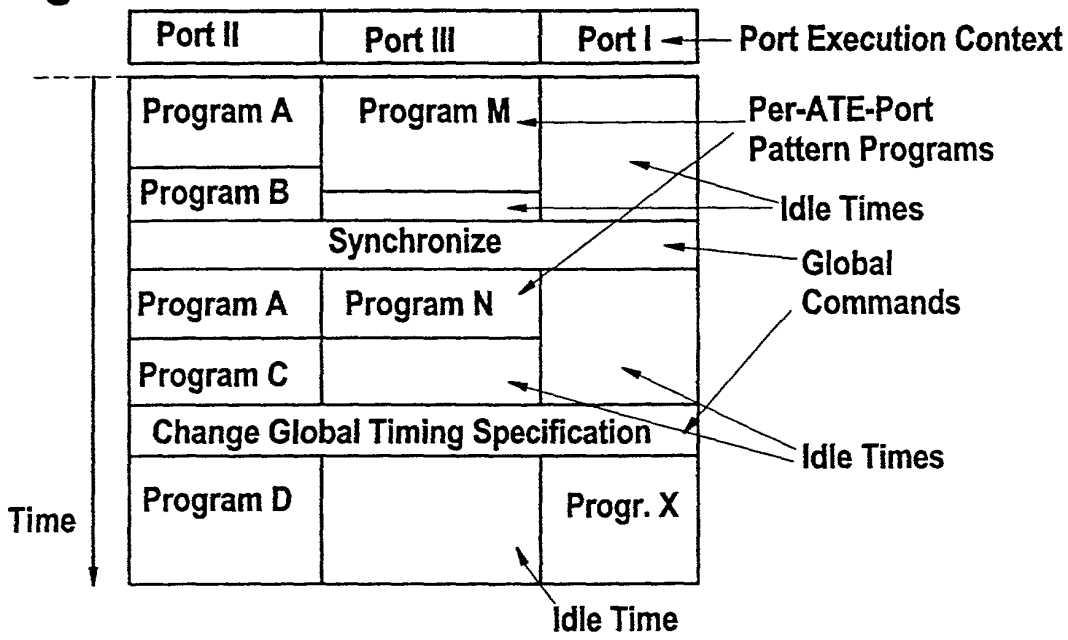
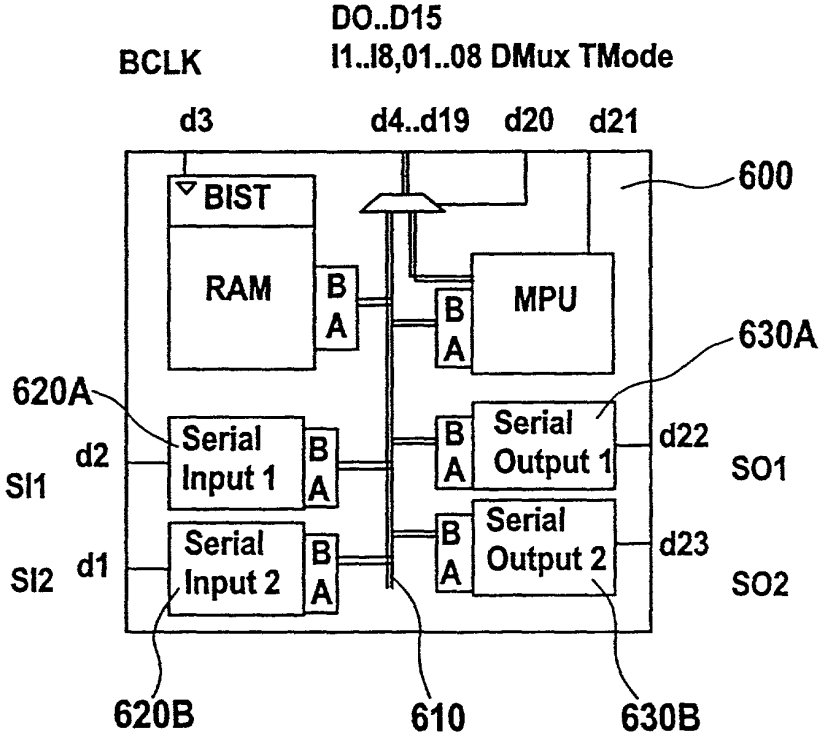

Port II
Port III
Port I
Port Execution Context
Program A
Program M
Per-ATE-Port
Pattern Programs
Program B
Idle Times
Synchronize
Global
Commands
Program A
Program N
Program C
Change Global Timing Specification
Idle Times
Time
Program D
Progr. X
Idle Time

Fig. 6


DO..D15
I1..I8,01..08 DMux TMode
BCLK
d3
d4..d19
d20
d21
600
BIST
RAM
B
A
MPU
630A
620A
Serial
Input 1
d2
SI1
Serial
Output 1
d22
SO1
Serial
Input 2
d1
SI2
Serial
Output 2
d23
SO2
620B
610
630B

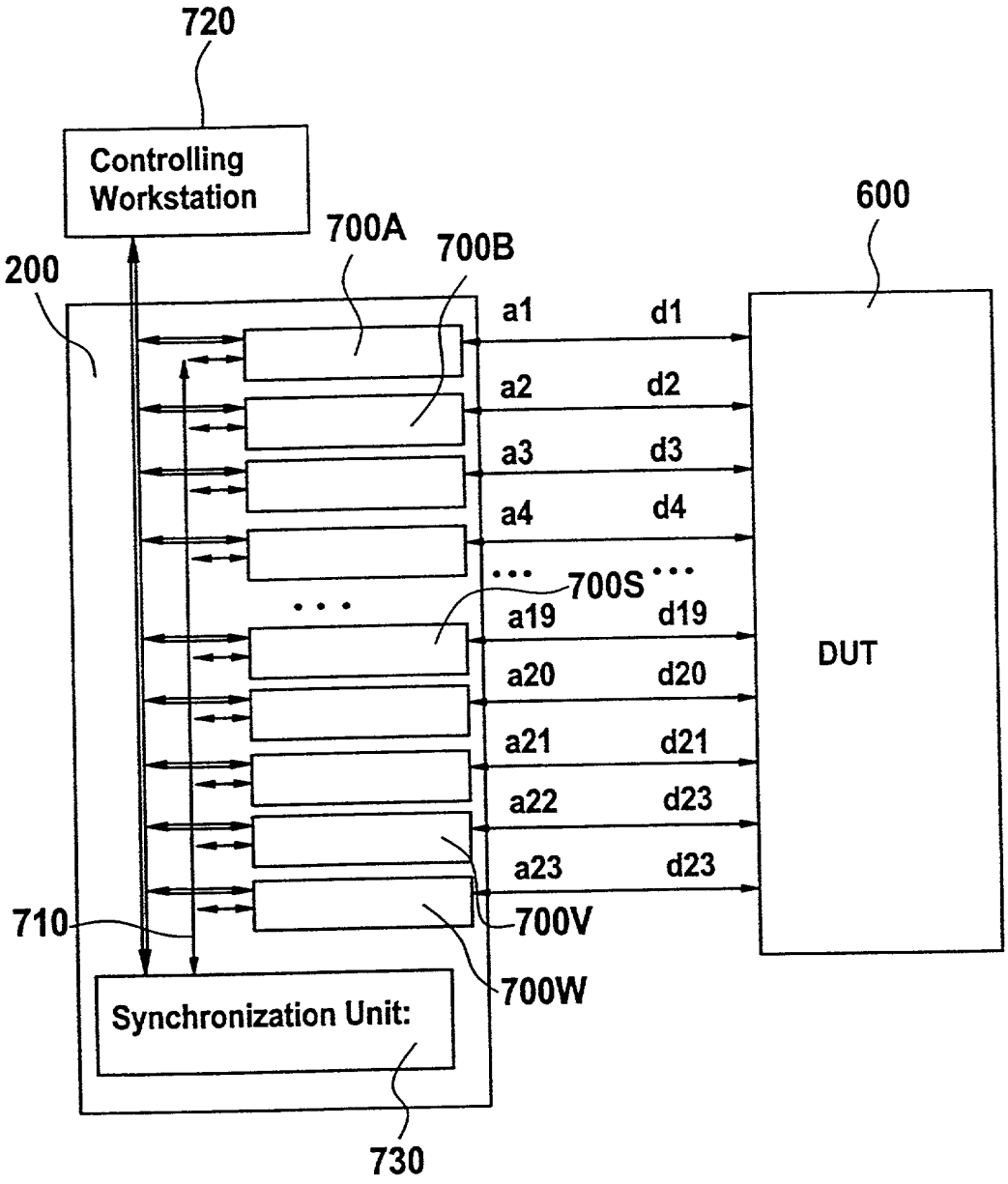

720
Controlling Workstation
600
700A
700B
200
a1
d1
a2
d2
a3
d3
a4
d4
700S
a19
d19
DUT
a20
d20
a21
d21
a22
d23
a23
d23
710
700V
700W
Synchronization Unit:
730

Fig. 7

Fig. 8

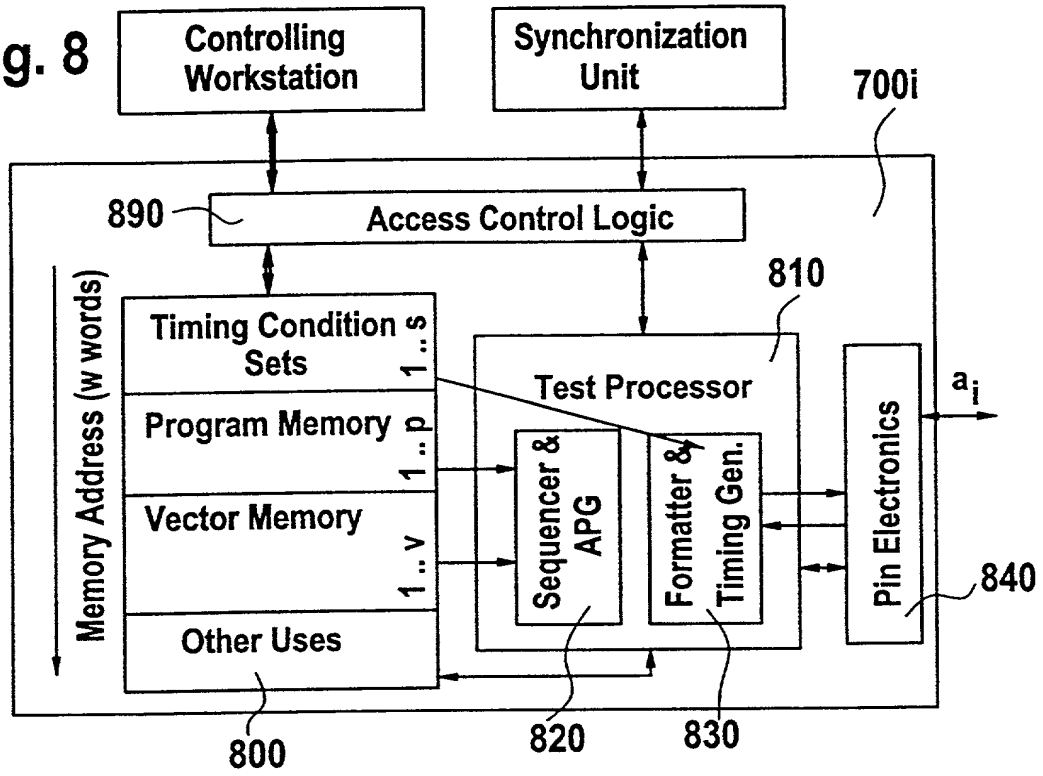
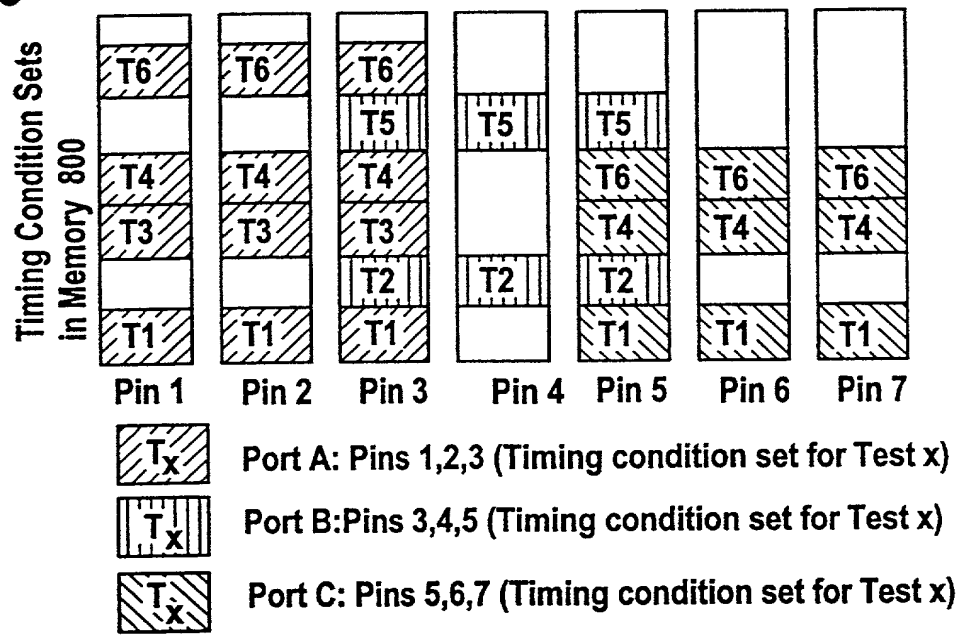

Controlling Workstation
Synchronization Unit
700i
890
Access Control Logic
810
Timing Condition Sets
1..s
Program Memory
1..p
Vector Memory
1..v
Other Uses
Memory Address (w words)
Test Processor
Sequencer & APG
Formatter & Timing Gen.
Pin Electronics
a_i
840
800
820
830

Fig. 9


Timing Condition Sets in Memory 800
T6
T5
T4
T3
T2
T1
Pin 1
Pin 2
Pin 3
Pin 4
Pin 5
Pin 6
Pin 7
Tx
Port A: Pins 1,2,3 (Timing condition set for Test x)
Port B:Pins 3,4,5 (Timing condition set for Test x)
Port C: Pins 5,6,7 (Timing condition set for Test x)

Vec #	Pins				Sequencer Instruction
	D0	...	D15	Dmux	
0	X	...	X	0	CORE 1"SI1_Data" CORE 2"SO1_Data"
1	p		p	1	LOOP 10000; COREDATA 1
2	X		X	1	
3	p		p	1	COREDATA 2
4	X		X	1	
					LOOP END

Fig. 10